In The Claims

Applicant submits below a complete listing of the current claims, including marked-up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing. This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims

1-37. Cancelled

38. (Currently Amended) A computer system comprising:

storage circuitry for holding a plurality of instructions at respective storage locations, the plurality of instructions including a first string of instructions including a set branch instruction indicating a target location within the storage circuitry at which a new instruction, not included in the first string, is stored, the first string further including a subsequent instruction that is subsequent in the first string to the set branch instruction;

instruction fetch circuitry to fetch instructions from said storage circuitry, the instruction fetch circuitry including a first instruction fetcher to fetch instructions, including the subsequent instructions~~instructions~~, from the first string and including a second instruction fetcher; and

execution circuitry to execute fetched instructions, including executing the set branch instruction,

wherein the second instruction fetcher is operative, responsive to execution of said set branch instruction, to fetch the new instruction from the location indicated by the set branch instruction, in parallel to the first instruction fetcher fetching the subsequent instruction.

39. (Previously Presented) The computer system according to claim 38, wherein the first string of instructions includes a condition instruction which defines a condition and defines that further instructions to be executed will include the new instruction only if the condition is satisfied.

40. (Previously Presented) The computer system according to claim 39, wherein the first string of instructions further includes an effect branch instruction for implementing a branch to the location indicated by the set branch instruction.

41. (Previously Presented) The computer system according to claim 40, the system further comprising select circuitry responsive to execution of the effect branch instruction to cause said execution circuitry to execute said new instruction if the condition defined by the condition instruction is satisfied.

42. (Previously Presented) The computer system according to claim 40, wherein said instruction fetch circuitry comprises two instruction buffers, a first buffer, connected to said execution circuitry, to hold the further instructions to be executed, and a second buffer to hold a second string of instructions including the new instruction, wherein the computer system includes circuitry to copy the contents of said second buffer into said first buffer responsive to execution of said effect branch instruction.

43. (Previously Presented) The computer system according to claim 40, wherein said instruction fetch circuitry comprises a third instruction fetcher for fetching instructions to implement predicted conditional instructions.

44. (Previously Presented) The computer system according to claim 38, wherein the target location holds an address of the new instruction, which is a first instruction of a string of new instructions to be fetched.

45. (Previously Presented) The computer system according to claim 38, wherein the branch instruction identifies a special register which holds an address from which a first instruction of a string of new instructions is to be fetched.

46. (Previously Presented) The computer system according to claim 38, wherein the target location holds an address of a memory location which holds an address of a first instruction of a string of new instructions to be fetched.

47. (Previously Presented) The computer system according to claim 38, further comprising decode circuitry for decoding said fetched instructions, said instruction fetch circuitry, decode circuitry and execution circuitry being arranged in a pipeline.

48. (Previously Presented) The computer system according to claim 40, wherein said effect branch instruction is located at a branch point after which said new instruction is to be executed.

49. (Cancelled)

50. (Previously Presented) The computer system according to claim 48, wherein the computer system comprises a branch point register for holding said branch point.

51. (Previously Presented) The computer system according to claim ~~38~~ 48, the computer system further comprising a return register for holding a return address being the address of the next instruction after said branch point, and wherein said set branch instruction identifies said return register to indicate the target location.

52. (Currently Amended) A method of operating a computer having storage circuitry holding a plurality of instructions at respective storage locations, said plurality of instructions being arranged in instructions strings including a first instruction string that includes a set branch instruction indicating a target location within the storage circuitry at which a new instruction, not included in the first string, is stored, the first string further including a subsequent instruction that is subsequent in the first instruction string to the set branch instruction, the method comprising:

fetching the subsequent instruction from said storage circuitry;

executing said set branch instruction; and

in response to executing said set branch instruction, fetching the new instruction from said storage circuitry in parallel to fetching the subsequent instruction.

53. (Previously Presented) The method according to claim 52, further comprising:

executing a condition instruction which defines a condition for a branch to be taken.

54. (Previously Presented) The method according to claim 53, wherein the plurality of instructions includes a second instruction string including the new instruction, wherein the method further comprises:

executing an effect branch instruction for implementing the branch;

in response to executing said set branch instruction, holding the indication of said target location in a target store, fetching in parallel instructions from the first instruction string and from the second instruction string commencing from said target location;

continuing to execute instructions from the first instruction string until the effect branch instruction is executed which indicates that further instructions to be executed are instructions from the second instruction string if the condition defined by the condition instruction is satisfied; and

responding to said effect branch instruction by commencing execution of said instructions of the second instruction string.

55. (Previously Presented) The method according to claim 54, further comprising:

holding said instructions of the first instruction string in a first buffer; and

holding said instructions of the second instruction string in a second buffer;; and

in response to execution of the effect branch instruction, copying the contents of said second buffer into said first buffer.

56. (Previously Presented) The method according to claim 54, wherein said instructions from the first instruction string are fetched by a first instruction fetcher and said instructions from the second instruction string are fetched by a second instruction fetcher, wherein the method further comprises:

selecting which of said first and second instruction fetchers supplies instructions for execution, based on said effect branch instruction.

57. (Previously Presented) The method according to claim 54, wherein the branch instruction identifies as the target location the address from which the first instruction of a string of new instructions is to be fetched.

58. (Previously Presented) The method of claim 41, wherein said select circuitry is operable to connect a selected one of said first and second instruction fetchers to said execution circuitry.

59. (Previously Presented) A computer system comprising:

storage circuitry for holding a plurality of instructions at respective storage locations, the plurality of instructions including a first string of instructions including a set branch instruction indicating a target location within the storage circuitry at which a new instruction, not included in the first string, is stored, the first string further including a subsequent instruction that is subsequent in the first string to the set branch instruction;

execution circuitry to execute fetched instructions, including executing the set branch instruction; and

means for fetching the subsequent instruction and the new instruction from the storage circuitry in parallel in response to execution of the set branch instruction.

60. (New) The computer system of claim 38, further comprising:

a decode circuit to receive and decode fetched instructions, including the set branch instructions, and to supply the decoded fetched instructions, including the decoded set branch instruction, to the execution circuitry.

61. (New) The method of claim 52, further comprising:

prior to executing the set branch instruction, decoding the set branch instruction.